

INTELLIGENT NETWORK INTERFACE DEVICE AND SYSTEM FOR ACCELERATING COMMUNICATION

Patent Number: WO0013091

Publication date: 2000-03-09

Inventor(s): BOUCHER LAURENCE B [US]; BLIGHTMAN STEPHEN E J [US]; CRAFT PETER K [US]; HIGGEN DAVID A [US]; PHILBRICK CLIVE M [US]; STARR DARYL [US]

Applicant(s): ALACRITECH CORP [US]; BOUCHER LAURENCE B [US]; BLIGHTMAN STEPHEN E J [US]; CRAFT PETER K [US]; HIGGEN DAVID A [US]; PHILBRICK CLIVE M [US]; STARR DARYL [US]

Requested Patent: EP1116118 (WO0013091)

Application Number: WO1998US24943 19981120

Priority Number (s): US19980141713 19980828

IPC Classification: G06F13/00

EC Classification: H04L29/06

Equivalents: AU1533399, CA2341211, DE1116118T, JP2002524005T

Cited Documents: US5751715; US5280477; US5448566; US5634127; US5758186; US5671355

Abstract

An intelligent network interface card or communication processing device (30) works with a host computer (20) for data communication. The device provides a fast-path (159) that avoids protocol processing for most messages, greatly accelerating data transfer and offloading time-intensive processing tasks from the host CPU (28). The host retains a fallback processing capability for messages that do not fit fast-path criteria, with the device providing assistance such as validation even for slow-path messages, and messages being selected for either fast-path or slow-path (158) processing. A context (50) for a connection is defined that allows the device to move data, free of headers, directly to or from a destination or source in the host. The context can be passed back to the host for message processing by the host. The device contains specialized hardware circuits that are much faster at their specific tasks than a general purpose CPU. A preferred embodiment includes a trio of pipelined processors (482, 484, 486) devoted to receive, transmit and utility processing, providing full duplex communication for four Fast Ethernet nodes.

Data supplied from the **esp@cenet** database - I2